REMARKS/ARGUMENTS

The Office Action of 11/10/2005 has been carefully considered. In response thereto, the specification has been amended as set forth above. Reconsideration in view of the foregoing amendments and the following remarks is respectfully requested.

Applicant notes the suggestion that headings be added to the specification. As such headings are not strictly required, as inasmuch as instances of case law have construed such headings to have a limiting effect, Applicant respectfully declines.

Claims 1-10 were rejected as being anticipated by Lee. The rejection states in part:

> [F]ig. 5 of Lee et al. discloses a method (Fig. 13) for coding information in an electronic circuit, said circuit (Fig. 5) comprising at least two electrically coupled signal paths (52, 54, 56) characterized in that the method comprises the steps of: determining (55) the relative delay between (paragraph 0035) signals propagating on said paths (52, 56, 54) when said signals make a transition from a first logic level to a second logic level (this is a intrinsic for determining delay of 55 because to determined the delay or time-differences between two signals, the delay measurement must be made at the rising edges or at falling edges of the two signals); and producing an output signal having a further logic level (ADJ) depending on the relative delay between said signals (52, 56).

This rejection is respectfully traversed.

Unlike the present invention, Lee relates to a delay equalization circuit. Given two signal paths each having an input signal (IS1, IS2), a transmission path and an output signal (OS1, OS2), the goal is the minimize delay between OS1 and OS2. The signal ADJ referred to in the Office Action is used to control a slave variable delay unit 68 to achieve this end. The signal ADJ, however, is not "an output signal having a further *logic level*." In one embodiment of Lee (Fig. 7), the signal ADJ is an analog signal. In another embodiment, the signal ADJ is a digital word. It would not have been obvious for such digital word to be only a single bit in length (thereby forming "an output signal having a further logic level"), as the apparatus is Lee would then not function properly.

Accordingly, claims 1 and 6 are believed to patentably define over the cited reference. Dependent claims 2-5 and 7-10 are also believed to add novel and

patentable subject matter to their respective independent claims. Withdrawal of the rejection and allowance of claims 1-10 is respectfully requested.

Please charge any fees other than the issue fee and credit any overpayments to Deposit Account 14-1270.

Respectfully submitted,

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